

**Submission Instructions:**

Please follow the submission instructions provided in assignment 1.

Additionally, please note that you must show all the details of your work. Submission without sufficient details will be rejected.

**Assignment Instructions:**

- Using the 2-way set associative D-cache depicted below; give the result of the following memory accesses. These memory accesses are byte references.

a. Write to AE	f. Read from F4
b. Read from AC	g. Write to F7
c. Write to B4	h. Read from 29
d. Read from C7	i. Write to 10
e. Write to D2	j. Read from 2A

Set-0											
TAG	D0	D1	D2	D3	D4	D5	D6	D7	V	D	LRU
1010	X	X	X	X	X	X	X	X	1	0	0
1011	X	X	X	X	X	X	X	X	0	1	1

  

Set-1											
TAG	D0	D1	D2	D3	D4	D5	D6	D7	V	D	LRU
1100	X	X	X	X	X	X	X	X	0	1	1
1101	X	X	X	X	X	X	X	X	1	0	0

- The result should be in the format of 'H:' (hit), 'CM:' (compulsory miss) or 'M:' (miss).
  - Use the LRU replacement policy; assuming that 0 denotes LRU and 1 denotes MRU.
  - If you replace a block, assume that only the tag is changed and the data (marked as X) is unchanged.
  - All numeric values are in hexadecimal.
- Consider a direct mapped memory hierarchy with the following specifications: The main memory is 64K bytes, the block size is 32 bytes, the cache is an I-cache, and it has 32 lines. Furthermore, initially all the blocks are invalid

For each of the following memory accesses determine whether it is a hit (H), compulsory miss (C), or non-compulsory miss (M). Explain your answer in sufficient details.

- |                    |                    |
|--------------------|--------------------|
| a. PC = CA12 _____ | f. PC = FE15 _____ |
| b. PC = CA13 _____ | g. PC = FE13 _____ |
| c. PC = CA23 _____ | h. PC = FE23 _____ |
| d. PC = CA14 _____ | i. PC = FE14 _____ |
| e. PC = CA24 _____ | j. PC = FE24 _____ |

3. Answer the following questions related to reference addresses:
- Given a 64-byte cache block, a 32 KB direct-mapped D-cache (assume byte-addressable), and a 32-bit address reference word, which bits of a reference word would be used for tag, index, and offset? How many bits per line will be saved in the cache?
  - Given a 128-byte cache block a set associative D-cache with 4 sets and 4 lines per set (assume byte-addressable), and a 24-bit address reference word, which bits of a reference word would be used for tag, index, and offset? Assuming an LRU replacement policy and assuming that the LRU bits for each line are saved inside the line, what is the total number of bits required for the entire cache?
4. Consider a memory hierarchy with two levels of cache ( $I_1$  and  $I_2$ ). The access time to the  $I_1$  cache is 10 nano-seconds, the access time to the  $I_2$  cache is 100 nano-seconds, and the access time to the Main Memory is 1 micro-second. The hit ratio in the  $I_1$  cache is 0.85 and the hit ration in the  $I_2$  cache is 0.9. Find the Expected Access time for this configuration.